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µTasker Document

µTasker – i.MX RT Power-Cycling Watchdog

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1. Introduction

The i.MX RT processors boot from a ROM LOADER, which reads the program's configuration from QSPI flash. Once the configuration has been identified as being valid the ROM LOADER will start execution of the user's program.

For this to operate reliably the QSPI flash must be operational and the ROM LOADER itself must be reliable. If either were not to be the case the ROM LOADER could remain in its operating mode (such as ISP [In System Programming]) and the user's code will not be started. Such a situation can result in the need for a power cycle in order to recover the system and can represent a serious issue in critical systems.

Practically some risks have been identified:
- the use of certain FlexRAM configurations by user programs can leave the ROM LOADER in an inoperative state (the ROM LOADER tends to require 64k of OCRAM to be available, for example)
- if there is a software or watchdog reset during a QSPI flash programming or erase operation the QSPI flash will temporarily be in a state where its content cannot be read and so the ROM LOADER will stay in the ISP mode and potentially never start the user program

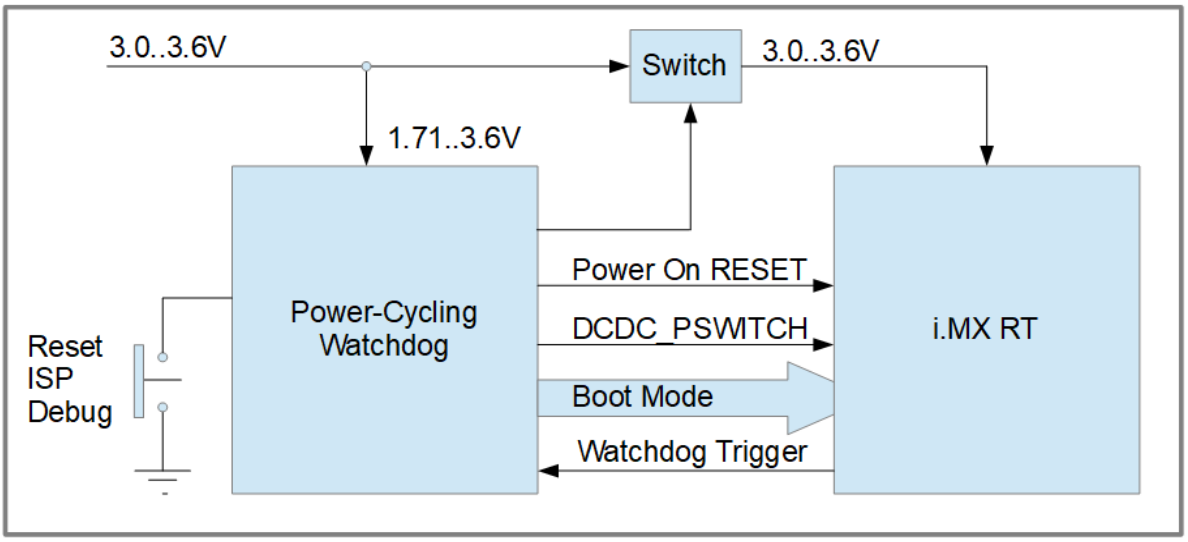
Since these represent risks requiring power cycling intervention to recover a method of providing such automatic recovery has been developed that can be used as a standard and cost effective HW approach to ensure high reliability with the i.MX RT parts in critical systems (or generally to ensure product quality).

In addition to solving the i.MX RT's potential booting weakness the solution also integrates other typical system requirements to give it the following feature list

- *small PCB real estate (the Kinetis KL3 in QFN16 is targeted)*
- *cost efficient*
- *very low power*
- *power-cycling watchdog to ensure system recovery due to above mentioned causes or latch-ups due to interference*
- *accurate power sequencing control of i.MX RT*
- *push button reset*
- *push button ISP reset to enter ISP mode without requiring DIP switches*
- *push button debug reset to temporarily disable the power-cycling watchdog (and i.MX RT watchdog) during debugging sessions*
- *optional I2C communication in order to request statistics/counters and command power down periods*
- *option to add further features by firmware*

Although i.MX RT 105x devices produced at the time of writing will have a silicon revision that has removed initial and critical HW errata it can't be excluded that stocks of older parts (A-revision) may need to be used in some circumstances. **These have some HW errata that can cause the parts to either not power up (DCDC start-up failure – see errata ERR011092) or to be potentially damaged by high in-rush current (see errate ERR011091).** The solution offers optional control of the needed sequences to avoid this when built with the project define `SUPPORT_MASK_A_EXACT_POWER_SEQUENCING`

2. Power Cycling Watchdog Block Diagram



The circuitry consists of the power-cycling watchdog, which is a Kinetis KL02Z8VFG4 or KL03Z8VFG4 (in miniature 3.0 x 3.0 x 0.65mm 16-pin QFN package) performing specific power cycling/sequencing steps, monitoring the correct operation of the i.MX RT and controlling its reset and boot mode according to user input from a *single* push button switch.

The switch can be a cheap low resistance p-channel MOSFET such as the DMG2305UX.

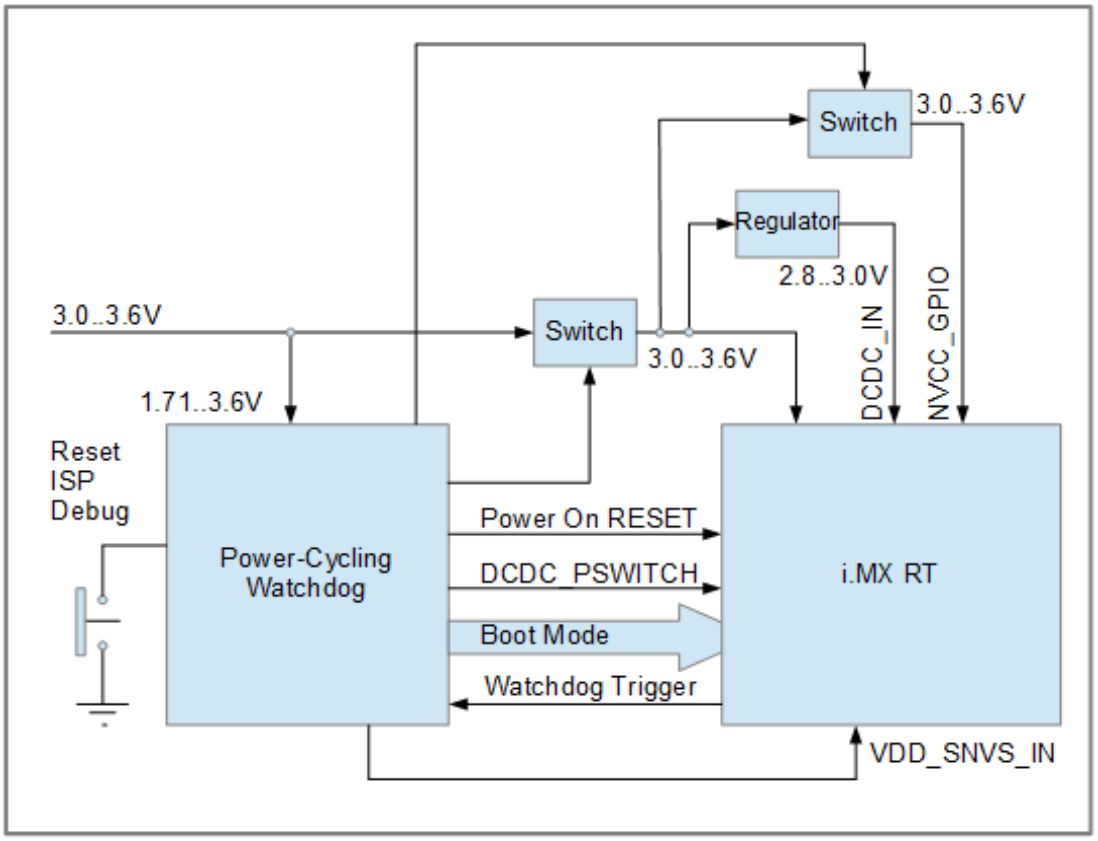
The power-cycling watchdog processor operates in a low power stop mode to achieve very low current consumption, waking only momentarily to service specific interrupts (push button switch presses, watchdog trigger edges and low power timers monitoring the correct operation of the i.MX RT).

The utilised KL02/KL03 parts require a minimum of external components (resistors and capacitors).

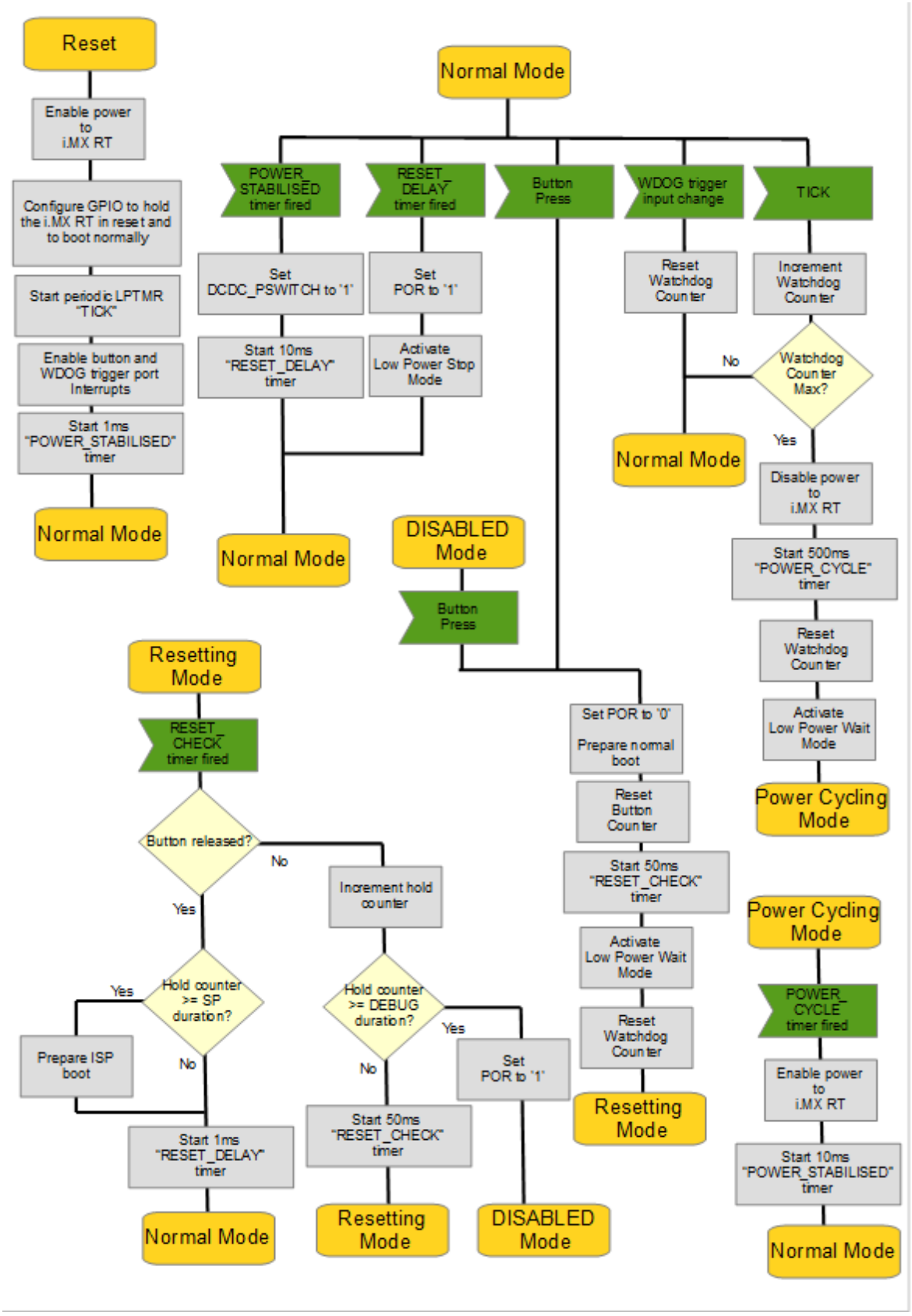
The KL02/KL03 firmware is included in the µTasker project and can be programmed to these devices either before they are assembled on the board or when mounted (requiring SWD connections).

The KL03 also supports in-circuit programming via I^2C or UART.

When HW errata workarounds are required there are two additional control lines used which control the sequencing of individual power rails as shown in the extended block diagram. One additional switch and an additional voltage regulator are shown which allow controlling the application of power to the GPIO supply and regulate the voltage level switched to the the DCDC input. A second supply control, VCC_SNVS_IN, is shown without a switch since it is a low current sink (maximum 250µA) that can be supplied by a KL02/KL03 port output directly.



3. Power Cycling Watchdog State Event Machine

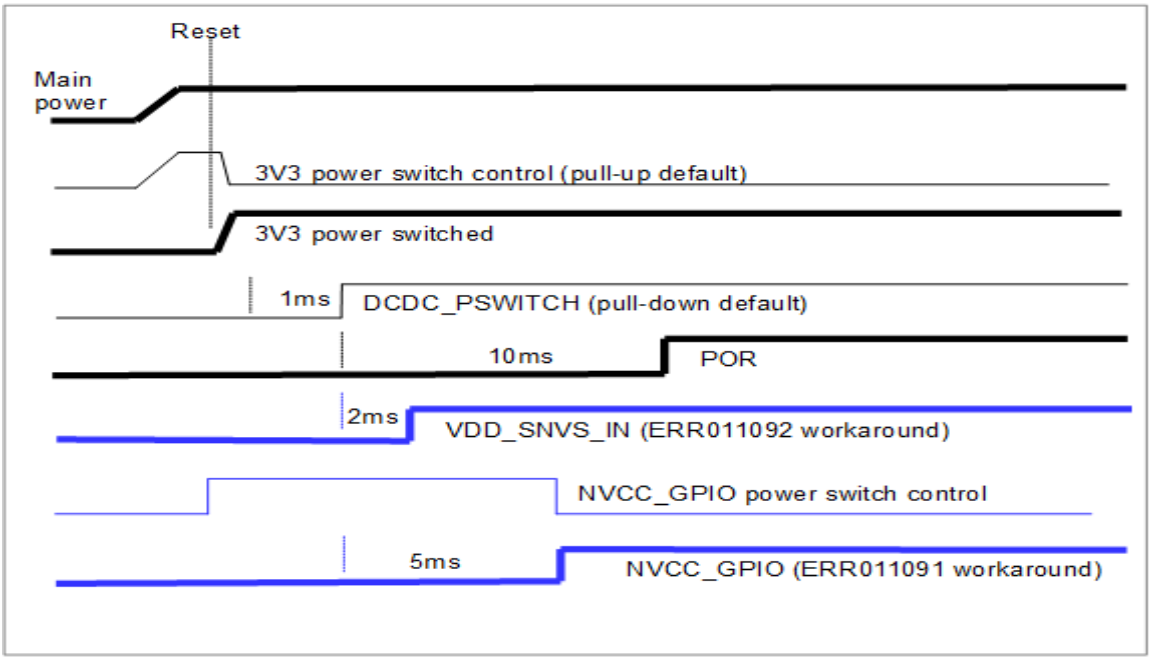


Typically the push button is used to perform a normal reset (guaranteeing > 50ms reset pulse) when pressed momentarily and held less that 3s.

When held longer that 6s the power-cycling watchdog monitoring is disabled until the next button press (or power cycle) so that developers can debug code on the i.MX RT device without the power cycling watchdog triggering a power cycle. Optionally a further output of the KL02/KL03 can be connected to an input on the i.MX RT in order to signal to it (during the reset sequence) whether it should enable or disable its own watchdog (to synchronise to the power cycling watchdog's mode of operation). This output is enabled by the define `SIGNAL_WDOG_STATE`.

A button press duration between 3 and 6s will result in the i.MX RT being reset to its ISP mode so that firmware can be loaded to it, or other ISP functions executed. *In this mode the power cycling watchdog operation is also disabled*. Since the ISP mode control of the i.MX RT involves controlling the logical state of two mode inputs at reset the solution simplifies the typical HW circuitry used to perform this (eg. no DIP switch is needed)

The power sequencing performed is shown in the following diagram:



As soon as the controller starts it enables the main power to be switched to the i.MX RT but doesn't enable the DCDC in the i.MX RT via the DCDC_PSWITCH input *until after a delay of 1ms* to allow it to first stabilise. During this time the i.MX RT is held in its reset state via the POR input and for a further 10ms to allow the DCDC output to become ready.

Each time the power cycling watchdog needs to power down the processor by removing the switched 3V3 power line it subsequently restarts the exact same sequent to re-power again.

In the case of hardware errata workarounds (the control is not shown in the state-event-diagram) the differences are that

– the input voltage to the DCDC converter is reduced to a range of 2.8..3.0V to work around errata ERR011093 (avoiding potential unexpected DCDC resets). *This is controlled by the power supply circuitry and not by the power-cycling watchdog.*

– VDD_SNVS_IN is delayed by 2ms from enabling the DCDC converter (*normally this voltage is applied before any other voltages and also removed as last voltage, but in the errata case battery backup is not possible when the internal DCDC converter is used*). This works around errata ERR011092 (ensuring that the DCDC converter starts).

– NVCC_GPIO is delayed by 5ms from enabling the DCDC converter. This works around errata ERR011091 (ensuring that there is no high in-rush current to the GPIO supply that could potentially cause damage to the device). *Note that this avoids the GPIO power rails being applied before the VDD_SOC_IN is present, whereby VDD_SOC_IN is the regulated 1.1V output of the on-chip DC/DC converter.*

DCDC converter output check

With the option `MONITOR_DCDC_OUTPUT` the COMPARATOR in the KL02/KL03 is used to monitor the DC/DC converter output voltage. If the DC/DC converter voltage doesn't turn on as expected during the power sequencing phase the sequence will be stopped and reattempted. If the DC/DC converter output should fail during operation it will result in a power sequence, whereby the GPIO supply is immediately interrupted when `SUPPORT_MASK_A_EXACT_POWER_SEQUENCING` is enabled in order to protect against potentially high currents when this occurs. This option is advised especially when a Rev. A i.MX RT 105x is being used!

> *It is to be noted that the KL02/KL03 refrains from applying any voltages to the connected i.MX RT until the power sequencing has been performed and the device is itself powered up. This is true in normal operation or when `SUPPORT_MASK_A_EXACT_POWER_SEQUENCING` is enabled.*

4. Additional Optional Features

If the define `I2C_COUNTERS` is enabled the power-cycling watchdog processor can be optionally connected to the i.MX RT processor that it is monitoring via its I²C interface, whereby the watchdog processor takes on the role of a slave device with the I²C addresses 0x28 for write and 0x29 for read (the address is configurable by using the define `IMXRT_WDOG_I2C_SLAVE_ADDRESS`). The i.MX RT can communicate as an I²C master in order to request information from the watchdog processor or to command it to perform certain operations.

Read Only Operations

The interface allows addressed registers to be read as follows (counters are reset when the watchdog processor is reset / power cycled):

`0x00..0x03` contains a 32-bit count value of the number of 200ms ticks the watchdog processor has been running for (allowing 27 years before roll-over).

`0x04..0x07` contains a 32-bit count value of the number of 200ms ticks the i.MX has been running for since it was last power cycled (due to power cycling watchdog firing).

`0x08..0x0b` contains a 32-bit count value of the number of 200ms ticks the i.MX has been running for since it was last reset.

`0x0c..0x0f` contains a 32-bit count value of the number of times the i.MX DC/DC converter failed to start.

0x10..0x13 contains a 32-bit count value of the number of times the i.MX has been power cycled.

0x14..0x17 contains a 32-bit count value of the number of times the i.MX has kicked the power cycling watchdog (since the watchdog processor started).

0x18..0x1b contains a 32-bit count value of the number of times the watchdog processor reset the i.MX due to the reset button being pressed.

0x1c..0x1f contains a 32-bit count value of the number of times the watchdog processor has reset the i.MX to debug mode.

0x20..0x23 contains a 32-bit count value of the number of times the watchdog processor has reset i.MX to ISP programming mode.

0x24..0x27 contains a 32-bit version number value (eg. 0x00010004 = V0.1.0.4)

Read/Write Operations

0x28..0x2b contains a 32 bit tick count-down value that can be read and written. If this is set to non-zero by the i.MX it will cause it to be powered up (if powered down) when it reaches 0. This should generally be written as a 4 byte write (see also note in following 0x5a command).

0x2c Command value that can be written with the following commands:

- 0x5a power down the i.MX RT processor and power up again when the count-down value reaches zero (*ignored if the count-down value is already zero*).
  It is possible to set the time and command the power down with a single I2C write if 5 bytes are written to the register address 0x28. The first 4 define the duration and the final one kicks off the command. For example 0x05 0x00 0x00 0x00 0x5a will power down for 1s.
- 0x82 commands a warm reset of the i.MX RT (50ms low pulse on the POR line)
- 0x83 commands a warm reset of the i.MX RT (50ms low pulse on the POR line) and exists in debug mode (with watchdogs disabled)
- 0x84 commands a warm reset of the i.MX RT (50ms low pulse on the POR line) and exists in ISP mode

If this address is read after issuing a command it will contain the result of the last command, which is the inverse of it of it was successful or the same value if not accepted. 0 will generally mean that no command has ever been issued.

5. Conclusion

The inclusion of the Power-Cycling Watchdog circuitry in all i.MX RT based products allows a cost effective method to ensure reliability in avoiding the potential situations when the ROM LOADER doesn't allow the user program to start.

Due to its additional features such as power sequencing and flexible ISP mode control by a single push button it also simplifies designs and can reduce overall parts count and costs over typical passive circuitry solutions.

Additional features like timed power down periods and counters indicating the overall reliability of operation further extend the usefulness of the design.

Modifications:

V1.00 17.5.2021 First version
V1.01 1.7.2021 Added errata workaround power sequencing option
V1.02 21.7.2021 Added extended features via I^2C
V1.03 17.3.2022 Added I2C version request and details about DC/DC output voltage monitoring option
V1.04 19.04.2022 Updated I2C interface