Strapping Options

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Pin Function</th></tr>
<tr><td>22
21
20</td><td>PHYAD2
PHYAD1
PHYAD0</td><td>Ipd/O
Ipd/O
Ipu/O</td><td>The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7.
The default PHY Address is 00001.
PHY Address bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>27
41
40</td><td>CONFIG2
CONFIG1
CONFIG0</td><td>Ipd/O
Ipd/O
Ipd/O</td><td>The CONFIG[2:0] strap-in pins are latched at power-up / reset and are defined as follows:
<table><tr><th>CONFIG[2:0]</th><th>Mode</th></tr><tr><td>000</td><td>MII (default)</td></tr><tr><td>001</td><td>RMII</td></tr><tr><td>010</td><td>SMII</td></tr><tr><td>011</td><td>Reserved – not used</td></tr><tr><td>100</td><td>PCS Loopback</td></tr><tr><td>101</td><td>RMII back-to-back</td></tr><tr><td>110</td><td>MII back-to-back</td></tr><tr><td>111</td><td>Reserved – not used</td></tr></table></td></tr>
<tr><td>29</td><td>ISO</td><td>Ipd/O</td><td>ISOLATE mode
Pull-up = Enable
Pull-down (default) = Disable
During power-up / reset, this pin value is latched into register 0h bit 10.</td></tr>
<tr><td>43
(KSZ8041TL)</td><td>SPEED</td><td>Ipu/O</td><td>SPEED mode
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.</td></tr>
<tr><td>43
(KSZ8041FTL)</td><td>SPEED /

no FEF</td><td>Ipu/O</td><td>If copper mode (FXEN=0), pin strap-in is SPEED mode.
Pull-up (default) = 100Mbps
Pull-down = 10Mbps
During power-up / reset, this pin value is latched into register 0h bit 13 as the Speed Select, and also is latched into register 4h (Auto-Negotiation Advertisement) as the Speed capability support.

If fiber mode (FXEN=1), pin strap-in is no FEF.
Pull-up (default) = Enable Far-End Fault
Pull-down = Disable Far-End Fault
This pin value is latched during power-up / reset.</td></tr>
</table>

Pin Number	Pin Name	Type(1)	Pin Function
23	DUPLEX	Ipu/O	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex During power-up / reset, this pin value is latched into register 0h bit 8 as the Duplex Mode.
42 **(KSZ8041TL)**	NWAYEN	Ipu/O	Nway Auto-Negotiation Enable Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12.
42 **(KSZ8041FTL)**	NWAYEN	Ipu/O	If copper mode (FXEN=0), pin strap-in is Nway Auto-Negotiation Enable. Pull-up (default) = Enable Auto-Negotiation Pull-down = Disable Auto-Negotiation During power-up / reset, this pin value is latched into register 0h bit 12. If fiber mode (FXEN=1), this pin configuration is always strapped to disable Auto-Negotiation.

Note:

1. Ipu/O = Input with internal pull-up (40K +/-30%) during power-up/reset; output pin otherwise.
   Ipd/O = Input with internal pull-down (40K +/-30%) during power-up/reset; output pin otherwise.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may drive high during power-up or reset, and consequently cause the PHY strap-in pins on the MII/RMII/SMII signals to be latched high. In this case, it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap-in to ISOLATE or PCS Loopback mode, or is not configured with an incorrect PHY Address.